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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/679,042	10/02/2000	Wajih Dalal	M-9497 US	4713

7590 06/23/2003

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EXAMINER

CHAUDRY, MUJTABA M

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 06/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/679,042

Applicant(s)

DALAL ET AL.

Examiner

Mujtaba K Chaudry

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-- **Th MAILING DATE of this communication app ars on the cover sheet with th correspondence address --**
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 October 2000.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☒ Claim(s) 2 and 4-7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 October 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other:

DETAILED ACTION

Drawings

The drawings are objected to because:

- In Figures 1-2 the margins need to be corrected such that the entire figure may be seen.
- A portion of Figure 2 is cut out due to the holes. The font size should be the same—12pt.
- The dark background effect in Figure 3 should be removed for clarity.
- In Figure 4, it is difficult and in some instances impossible to read what is written or shown.
- Essentially, formal drawings are required with proper margins and viewable information.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

- In the brief description of the drawings, the description for Figure 4 needs to be restated such that it includes the gist of the present application.

Appropriate correction is required.

Claim Objections

Claim 2 is objected to because of the following informalities:

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- The phrase "...testing components..." is not specific enough. Applicant should elaborate.

Claims 4-7 are objected to because of the following informalities:

- The preamble of the independent claim states, "the method comprising..." which is not appropriate. It needs to state what the method is for. The Examiner would like to point out that the preamble before the preliminary amendment was acceptable.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear where the testing takes place.

Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear if the output of the integrated circuit has a frequency. Claim needs to be rewritten clearly.

Claim 4 recites the limitation "integrated circuit tested" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turnquist et al. (USPN 6532561 B1).

As per claims 1 and 4, Turnquist et al. (herein after: Turnquist) substantially teaches (title and abstract) a method and apparatus that is configured to test a device under test (DUT) by supplying test signals to the DUT and evaluating an output of the DUT at a timing of a strobe signal. The test system (shown in Figure 3) includes an event memory for storing timing data of each event formed with an integer multiple of a reference clock period and a fraction of the reference clock period wherein the timing data represents a time difference between a current event and a reference point. An address sequencer is used for generating address data for accessing the event memory and a timing count and scaling logic are used for generating an event start signal. The event generation unit generates each event based on the event start signal and data indicating the fraction of the reference clock period. A host computer controls the overall operation of the event based test system. Turnquist also teaches (col. 6, lines 7-26) the event generation unit 34 to generate the events based on the overall timing data from the timing count and scaling logic 33. The events, which are the rising and falling points of test signals and

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strobe signals, generated are provided to the DUT 38 through the pin electronics 36. The pin electronics 36 includes a large number of interface circuits for interfacing between the semiconductor test system and the semiconductor device to be tested. Each interface circuit is formed of a driver and a comparator as well as switches (or relays) to establish input and output relationships with respect to the driver, comparator and the DUT 38. An example of circuit structure in the event generation unit 34 is shown in a circuit diagram of FIG. 8. Turnquist teaches (Figure 8) a latch with a clock signal (analogous to strobe element in the present application). Figure 8 also shows a plurality of fan out elements.

Turnquist does not explicitly teach a plurality of relays connected to the integrated circuit under test as stated in the present application.

However, Turnquist teaches (figure 8) a plurality of switches within the pin electronic unit 36, shown in Figure 3. Furthermore, the Examiner would like to point out that the pin electronic unit is connected to the integrated circuit being tested or DUT 38. The pin electronics unit 36 taught by Turnquist includes switches that are analogous to plurality of relays of the present application. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the plurality of switches within the test apparatus of Turnquist with a plurality of relays. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that a relay is essentially a controlled switch.

As per claims 2 and 3, Turnquist substantially teaches (Figures 5 and 12B), in view of above rejections, the test data to have various frequencies. In Figure 12B, the vernier data memory 72 stores four (4) vernier data per clock count memory location. Thus, the vernier data

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memory 72 has 40-bit width. This approach may be useful when a test vector contains many events that are less than one reference clock period. Combining the vernier data of two or more events allows the test system to operate at faster frequency than the system clock frequency, because two or more events can be produced at the same time based on the vernier data at each access (clock) of the event memory. Since the first word of each event count data contains the number of events to be generated, it is possible to identify the correct vernier data for the current event.

As per claims 5-7, Turnquist substantially teaches (claim 1), in view of above rejections, a event memory for storing timing data of each event formed with an integer multiple of a reference clock period (integral part data) and a fraction of the reference clock period (fractional part data) and event type data representing a type of each event to be generated by said event based test system. The timing data being a time difference between a current event and a predetermined reference point and an address sequencer for generating address data for accessing said event memory to read out said timing data therefrom. An event count logic for generating an event start signal, which is delayed by the reference clock period multiplied by the integral part data. A decompression unit provided between said event memory and said event count logic for reproducing event data from compressed event data stored in said event memory. An event generation unit for generating each event based on said event start signal from said event count logic and the fractional part data and said event type data from said event memory for formulating said test signal or strobe signals and a host computer for controlling an overall operation of said event based test system.

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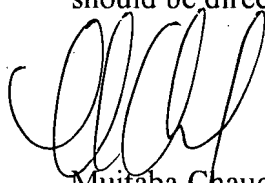
Conclusion

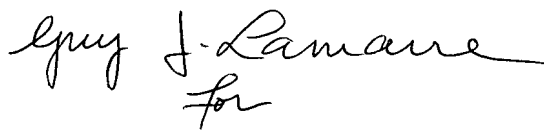
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Turnquist teaches a method and apparatus that is configured to test a device under test (DUT) by supplying test signals to the DUT and evaluating an output of the DUT at a timing of a strobe signal. Applicant is invited to review/read additional pertinent prior art has been included with this Office Action.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.


Mujtaba Chaudry
Art Unit 2133
June 10, 2003


for
Albert DeCady
Primary Examiner